Amendments

In the Claims:

Claims 1 and 2 (Canceled).

3. (Currently Amended) ~~The nonvolatile ferroelectric memory device of claim 2,~~ A nonvolatile ferroelectric memory device, comprising:

a memory control block for outputting control signals in response to a write enable command signal, a read enable command signal and a reset signal, wherein the control signals control data read/write operations;

a ferroelectric memory cell array for writing data and reading data stored in a sense amplifier in response to the control signals, the ferroelectric memory cell array comprising:

a plurality of bitline pairs;

a plurality of first single port memory cells connected in a column direction between bitline pairs; and

the sense amplifier connected between one of the plurality of bitline pairs; and

a power-up reset circuit for outputting the reset signal to restore data stored in the ferroelectric memory cell array,

wherein the plurality of first single port memory ~~cell comprises~~ cells comprise:

a first latch means for amplifying a high level by ~~using the~~ using a voltage difference among output nodes;

a write control means for selectively connecting the plurality of bitlines to output nodes in response to the control ~~signal~~ signals;

a storage means including a plurality of ferroelectric capacitors;

a second latch means for amplifying a low level by using the voltage difference among output nodes;

a pull-up switch for selectively applying a power supply voltage to the first latch means in response to the control ~~signal~~ signals; and

a pull-down switch for selectively connecting the second latch means to a ground voltage in response to the control ~~signal~~ signals.

4. (Original) The nonvolatile ferroelectric memory device of claim 3, wherein the first latch means comprises cross-coupled PMOS transistors between the output nodes.

5. (Currently Amended) The nonvolatile ferroelectric memory device of claim 3, wherein the storage means comprises:

first and second ferroelectric capacitors having one terminal connected to the output nodes respectively and the other terminal commonly receiving the control signals ~~signal~~; and

third and fourth ferroelectric capacitors having one terminal connected to the output nodes respectively and the other terminal connected ~~to a ground~~ to the ground voltage.

6. (Currently Amended) The nonvolatile ferroelectric memory device of claim 5, wherein ~~the number~~ a number of the third and fourth ferroelectric capacitors increases according to ~~the loading~~ a loading level of the output nodes.

7. (Currently Amended) ~~The nonvolatile ferroelectric memory device of claim 1,~~ A nonvolatile ferroelectric memory device, comprising:

a memory control block for outputting control signals in response to a write enable command signal, a read enable command signal and a reset signal, wherein the control signals control data read/write operations;

a ferroelectric memory cell array for writing data and reading data stored in a sense amplifier in response to the control signals; and

a power-up reset circuit for outputting the reset signal to restore data stored in the ferroelectric memory cell array,

wherein the ferroelectric memory cell array comprises:

a plurality of bitline pairs;

a plurality of common pull-up lines;

a plurality of common pull-down lines;

a plurality of pull-up means for selectively applying a power supply voltage to the plurality of common pull-up lines respectively in response to the control signals ~~signal~~;

a plurality of pull-down means for selectively connecting the plurality of common pull-down lines with ground voltages respectively in response to the control signals ~~signal~~;

a plurality of second single port memory cells connected ~~in column~~ in a column direction between ~~a pair of the bitlines~~ bitline pairs; and

the sense amplifier connected between one of the plurality of bitline pairs.

8. (Currently Amended) The nonvolatile ferroelectric memory device of claim 7, wherein the plurality of second single port memory cells comprise ~~cell comprises~~:

a first latch means for amplifying a high level by using ~~the voltage~~ a voltage difference between output nodes;

a write control means for selectively connecting the plurality of bitlines to output nodes in response the control signals ~~signal~~;

a storage means including a plurality of ferroelectric capacitors; and

a second latch means for amplifying a low level by using the voltage difference between output nodes.

9. (Original) The nonvolatile ferroelectric memory device of claim 8, wherein the first latch means comprises cross-coupled PMOS transistors between the output nodes.

10. (Currently Amended) The nonvolatile ferroelectric memory device of claim 8, wherein the storage means comprises:

first and second ferroelectric capacitors having one terminal connected to the output nodes respectively and the other terminal commonly receiving the control signals ~~signal~~; and

third and fourth ferroelectric capacitors having one terminal connected to the output nodes respectively and the other terminal connected to a ground voltage.

11. (Currently Amended) The nonvolatile ferroelectric memory device of claim 10, wherein ~~the number~~ a number of the third and fourth ferroelectric capacitors is increased according to ~~the loading~~ a loading level control of the output nodes.

12. (Currently Amended) ~~The nonvolatile ferroelectric memory device of claim 1,~~ A nonvolatile ferroelectric memory device, comprising:

a memory control block for outputting control signals in response to a write enable command signal, a read enable command signal and a reset signal, wherein the control signals control data read/write operations;

a ferroelectric memory cell array for writing the data, and reading data stored in a sense amplifier in response to the control signals; and

a power-up reset circuit for outputting the reset signal to restore data stored in the ferroelectric memory cell array,

wherein the ferroelectric memory cell array comprises:

a plurality of write bitline pairs;

a plurality of read bitline pairs;

a plurality of first multi port memory cells connected ~~in column~~ in a column direction between one of the plurality of write bitline pairs and one of the plurality of read bitline pairs;

a write driving means connected between one of the plurality of write bitline pairs; and

~~a sense~~ the sense amplifier connected between one of the plurality of read bitline pairs.

13. (Currently Amended) The nonvolatile ferroelectric memory device of claim 12, wherein the plurality of first multi port memory cells comprise ~~cell comprises~~:

a first latch means for amplifying a high level by using ~~the voltage~~ a voltage difference between output nodes;

a plurality of write control means for selectively connecting the plurality of write bitline pairs to output nodes in response to the control signals ~~signal~~;

a storage means including a plurality of ferroelectric capacitors;

a second latch means for amplifying a low level by using the voltage difference between output nodes;

a plurality of read control means for changing a voltage level of the plurality of read bitline pairs in response to the control signals ~~signal~~ and a potential of the output nodes;

a pull-up switch for selectively applying a power supply voltage to the first latch means in response to the control signals ~~signal~~; and

a pull-down switch for selectively connecting the second latch means to a ground voltage in response to the control signals ~~signal~~.

14. (Original) The nonvolatile ferroelectric memory device of claim 13, wherein the first latch means comprises cross-coupled PMOS transistors between the output nodes.

15. (Currently Amended) The nonvolatile ferroelectric memory device of claim 13, wherein the storage means comprises:

first and second ferroelectric capacitors having one terminal connected to the output nodes respectively and the other terminal commonly receiving the control signals ~~signal~~; and

third and fourth ferroelectric capacitors having one terminal connected to the output nodes respectively and the other terminal connected ~~to a ground~~ to the ground voltage.

16. (Currently Amended) The nonvolatile ferroelectric memory device of claim 15, wherein ~~the number~~ a number of the third and fourth ferroelectric capacitors is increased according to ~~the loading~~ a loading level of the output nodes.

17. (Currently Amended) The nonvolatile ferroelectric memory device of claim 13, wherein the plurality of read control means comprises first and second switch means for selectively connecting the plurality of read bitline pairs to ground voltages in response to the control ~~signal~~ signals and a potential of the output nodes.

18. (Currently Amended) The nonvolatile ferroelectric memory device of claim 12, wherein the sense amplifier comprises:

a pull-up driving means for selectively applying a power supply voltage to the plurality of read ~~bitlines~~ bitline pairs according to ~~the voltage~~ a voltage difference of the read bitline pairs; and

a latch means storing data loaded on ~~the read bitline~~ read bitlines for a predetermined time.

19. (Currently Amended) The nonvolatile ferroelectric memory device of claim 18, wherein the pull-up driving means comprises:

a detecting means for detecting the voltage difference of the read bitline pairs; and

first and second pull-up means for ~~applying a power~~ applying the power supply voltage to the plurality of read bitline pairs respectively in response to an output signal from the detecting means.

20. (Currently Amended) ~~The nonvolatile ferroelectric memory device of claim 1,~~ A nonvolatile ferroelectric memory device, comprising:

a memory control block for outputting control signals in response to a write enable command signal, a read enable command signal and a reset signal, wherein the control signals control data read/write operations;

a ferroelectric memory cell array for writing the data, and reading data stored in a sense amplifier in response to the control signals; and

a power-up reset circuit for outputting the reset signal to restore data stored in the ferroelectric memory cell array;

wherein the ferroelectric memory cell array comprises:

a plurality of write bitline pairs;

a plurality of read bitline pairs;

a plurality of common pull-up lines;

a plurality of common pull-down lines;

a plurality of pull-up means for selectively applying a power supply voltage to the plurality of common pull-up lines respectively in response to the control signals ~~signal~~;

a plurality of pull-down means for selectively connecting the plurality of common pull-down lines to ground voltages respectively in response to the control signals ~~signal~~;

a plurality of second multi port memory cells connected ~~in column~~ in a column direction between one of the plurality of write bitline pairs and one of the plurality of read bitline pairs;

a write driving means connected between one of the plurality of write bitline pairs; and

~~a sense~~ the sense amplifier connected between one of the plurality of read bitline pairs.

21. (Currently Amended) The nonvolatile ferroelectric memory device of claim 20, wherein the second multi port memory cell comprises:

a first latch means for amplifying a high level by using ~~the voltage~~ a voltage difference between output nodes;

a plurality of write control means for selectively connecting ~~the bitlines~~ bitlines with output nodes in response to the control signals ~~signal~~;

a storage means including a plurality of ferroelectric capacitors;

a second latch means for amplifying a low level by using the voltage difference between output nodes; and

a plurality of read control means for changing a voltage level of the plurality of read bitline pairs ~~pair~~ in response to the control signals ~~signal~~ and a potential of the output nodes.

22. (Original) The nonvolatile ferroelectric memory device of claim 21, wherein the latch means comprises PMOS transistors cross-coupled between the output nodes.

23. (Original) The nonvolatile ferroelectric memory device of claim 21, wherein the storage means comprises:

first and second ferroelectric capacitors having one terminal connected to the output nodes respectively and the other terminal commonly receiving the control signals ~~signal~~; and

third and fourth ferroelectric capacitors having one terminal connected to the output nodes respectively and the other terminal connected to a ground voltage.

24. (Currently Amended) The nonvolatile ferroelectric memory device of claim 22, wherein ~~the number~~ a number of the third and fourth ferroelectric capacitors increases according to ~~the loading~~ a loading level of the output nodes.

25. (Currently Amended) The nonvolatile ferroelectric memory device of claim 20, wherein the sense amplifier comprises:

a pull-up driving means for selectively applying a power supply voltage to the plurality of read bitline ~~bitlin~~ pairs according to a voltage ~~the voltage~~ difference of the plurality of read bitline pairs; and

a latch means for storing data loaded on ~~the read~~ read bitlines for a predetermined time.

26. (Currently Amended) The nonvolatile ferroelectric memory device of claim 25, wherein the pull-up driving means comprises:

a detecting means for detecting the voltage difference of the plurality of read bitline pairs; and

first and second pull-up means for applying ~~a power~~ the power supply voltage to the plurality of read bitline pairs respectively in response to an output signal from the detecting means.